

Amendments to the Claims

1. (*Currently Amended*) A phase comparator, ~~particularly~~ for a PLL module, that compares the phase angle of a first input signal with a second input signal by evaluating the edges of the input signals and generates reset signals therefrom, characterized in that at least one additional circuit (~~4, 5~~) is provided that evaluates further, different edges of the input signal or signals (~~SIG, COMP~~) and generates therefrom additional reset signals (~~CLR_N~~) for the regulating signal or signals (~~UP, DOWN~~).
2. (*Currently Amended*) A phase comparator as claimed in claim 1, characterized in that the phase comparator obtains the regulating signals from the rising/decaying edges (~~a, b~~) of the input signals (~~SIG, COMP~~) and in that the additional circuit (~~4, 5~~) derives the additional reset signals (~~CLR_N~~) from the decaying/rising edges (~~c, d~~) of the input signals (~~SIG, COMP~~).
3. (*Currently Amended*) A phase comparator ~~as claimed in any of the foregoing claims~~, as claimed in claim 1, characterized in that a dedicated additional circuit (~~4, 5~~) is provided for each of the two input signals, with one additional circuit (~~4~~) evaluating the edges of the first input signal (~~SIG~~) and the second additional circuit (~~5~~) evaluating the edges of the second input signal (~~COMP~~).
4. (*Currently Amended*) A phase comparator ~~as claimed in any of the foregoing claims~~, as claimed in claim 1, characterized in that one additional circuit (~~4~~) evaluates the rising (~~a~~) and decaying (~~c~~) edges of one input signal (~~SIG~~) and the other additional circuit (~~5~~) evaluates the rising (~~b~~) and decaying (~~d~~) edges of the other input signal (~~COMP~~).
5. (*Currently Amended*) A phase comparator ~~as claimed in any of the foregoing claims~~, as claimed in claim 1, characterized in that the output signals (~~A, B~~) from the additional circuits (~~4, 5~~) are applied to the reset inputs (~~CLR_N~~) of flip-flops (~~1, 2~~) belonging to the phase comparator via a gate (~~15~~), there also being connected to the gate (~~15~~) a gate (~~3~~) to which the regulating signals (~~UP, DOWN~~) are applied.

6. (*Currently Amended*) A phase comparator ~~as claimed in any of the foregoing claims, as~~
claimed in claim 1, characterized in that the additional circuits ~~(4, 5)~~ each have two RS
flip-flops ~~(6, 7 and 6', 7' respectively)~~ and gates ~~(8 to 14 and 8' to 14' respectively)~~, which
are integrated into the PLL circuit.

7. (*Currently Amended*) A phase comparator ~~as claimed in claim 1 or 2, as claimed in~~
claim 1, characterized in that the two input signals ~~(SIG, COMP)~~ are applied to the
additional circuit ~~(4 or 5)~~ via an OR gate.